



55W, 28V High Power RF LDMOS FETs

Description

The ITDH09055E2 is a 55-watt, unmatched LDMOS FETs, designed for Wide-band and Mobile radio applications with frequencies from 1 to 1000 MHz. It can be used in Class AB/B and Class C for all typical modulation formats.



• Typical Performance (On Innegration fixture with device soldered):

VDD = 28 Volts, IDQ = 100 mA, Pulse CW, Pulse Width = 10us, Duty Cycle = 12%.

Frequency	Gp (dB)	P _{-1dB} (W)	$\eta_D@P_{-1}$ (%)	P _{-3dB} (W)	$\eta_D@P_{-3}$ (%)
1000 MHz	19	50	55	55	58

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative for Improved Class C Oper.
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+95	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _C = 85°C, T _J =200°C, DC test	R _{θJC}	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics Drain-Source Voltage V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}	95	—		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA



Gate--Source Leakage Current ($V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{ V}$, $I_D = 300\ \mu\text{A}$)	$V_{GS(th)}$	—	2.15	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{ V}$, $I_D = 100\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	3.0	—	V

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1000\text{ MHz}$, Pulse Width = 10us, Duty Cycle = 12%..

Power Gain	G_p	—	19	—	dB
Drain Efficiency@P3dB	η_D	—	58	—	%
3 dB Compression Point	P_{-3dB}	—	55	—	W
Input Return Loss	IRL	—	-10	—	dB

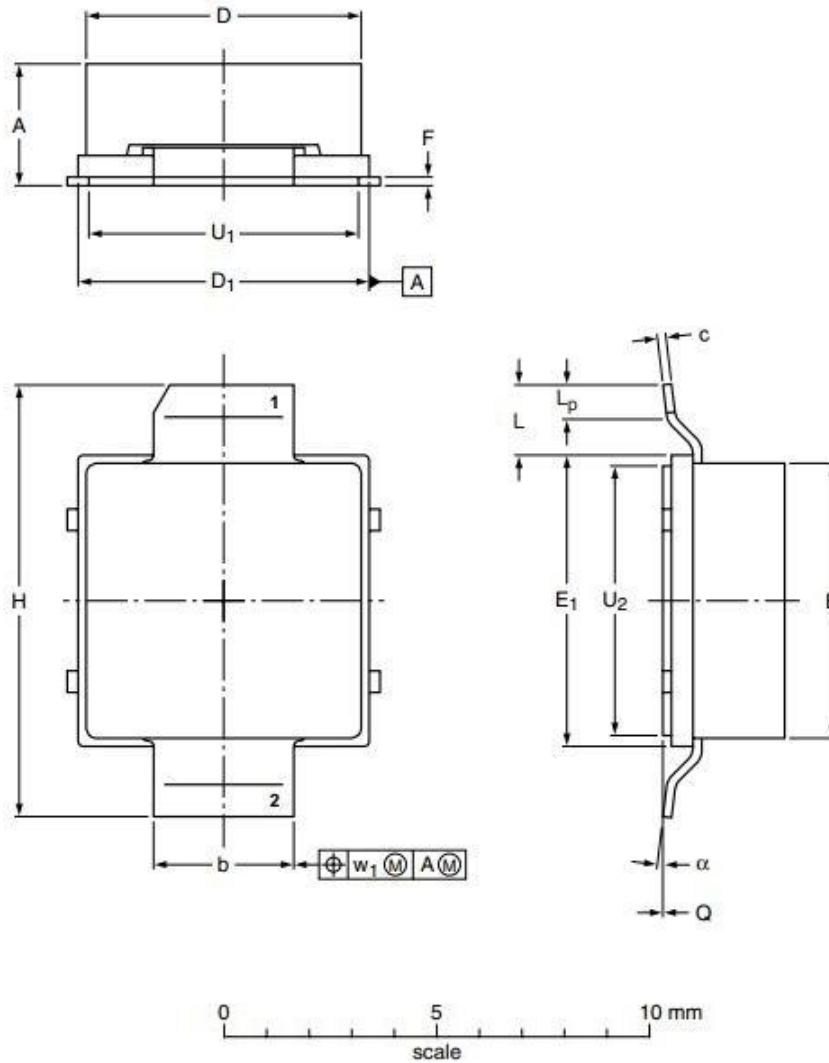
Load Mismatch (In Innogrator Test Fixture, 50 ohm system): $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 1000\text{ MHz}$

VSWR 10:1 at 55W pulse CW Output Power	No Device Degradation
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Package Outline

Earless Flanged ceramic package; 2 leads (1-Drain、2-Gate、Flange-GND)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	L _p	Q	U ₁	U ₂	w ₁	α
mm	3.63	3.38	0.23	6.55	6.93	6.55	6.93	0.23	10.29	1.65	1.02	+0.05	6.43	6.43	0.51	7°
	3.05	3.23	0.18	6.40	6.78	6.40	6.78	0.18	10.03							
inches	0.143	0.133	0.009	0.258	0.273	0.258	0.273	0.009	0.405	0.065	0.040	+0.002	0.253	0.253	0.02	7°
	0.120	0.127	0.007	0.252	0.267	0.252	0.267	0.007	0.395							

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-E2A					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/3/16	Rev 1.0	Product Datasheet

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